AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS:

1. (Currently amended) A method of adjusting ~~the~~ a loop gain constant in a phase-lock loop (PLL) synthesizer having a controllable oscillator, comprising the steps of:

(a) using a first PLL loop gain constant (α_1) during ~~the~~ a phase/frequency acquisition mode of the PLL synthesizer; and

(b) performing the following two steps when the PLL synthesizer transitions from the phase/frequency acquisition mode into ~~the~~ a tracking mode:

(b1) adding a DC offset to the PLL synthesizer's controlled oscillator-tuning signal; and

(b2) changing the first PLL loop gain constant (α_1) to a second PLL loop gain constant (α_2) which is smaller in value than the first PLL loop gain constant (α_1).

2. (Original) A method as defined in claim 1, wherein the PLL synthesizer comprises a digital PLL synthesizer.

3. (Currently amended) A method as defined in claim 1, wherein ~~the~~ a normalized loop gain ratio (α_1/α_2) is restricted to power-of-two values.

4. (Original) A method as defined in claim 1, wherein steps (b1) and (b2) are performed during the same clock cycle.

5. (Original) A method as defined in claim 2, wherein the PLL synthesizer has a phase detector that provides a phase error comprising a reference phase R_R, and a variable phase R_V and comprising the further step of:

(c) making R_R equal to R_V in order to bring an uncorrected phase error (ϕ) provided by a phase detector equal to zero.

6. (Currently amended) A method as defined in claim 5, wherein the DC offset added in step (b1) is equal to $(\alpha_1/\alpha_2) * \phi_1$, wherein ($\phi_1$) is ~~the~~ a value of the uncorrected phase error (ϕ) provided by the phase detector at the instance the phase detector goes from the phase acquisition mode to the tracking mode (gear shift).

7. (Original) A method as defined in claim 5, wherein step 5(c) is performed in the same clock cycle as steps (b1) and (b2).

8. (Original) A method as defined in 5, wherein step (c) is performed by loading the variable phase (R_V) value into a reference register used to store the reference phase (R_R) value.

9. (Original) A method as defined in claim 8, wherein step (c1) is performed during the same clock cycle as steps (b1) and (b2).

10. (Currently amended) A method as defined in claim 9, further comprising the step of:

(d) performing ~~the~~ a regular adjustment using a frequency control word (FCW).

11. (Original) A method as defined in claim 1, wherein in step (b1) the PLL synthesizer's controlled oscillator-tuning signal comprises a phase error signal provided by a phase detector.

12. (Currently amended) A method as defined in claim 11, wherein the DC offset added in step (b1) equals $\Delta\phi = [(\alpha_1/\alpha_2) - 1] * \phi_1$, wherein ($\phi_1$) is ~~the~~ a value of ~~a~~ the uncorrected phase error signal provided by ~~a~~ the phase detector at the instance the phase detector goes from the phase acquisition mode to the tracking mode (gear shift).

13. (Currently amended) A PLL synthesizer, comprising:

a phase detector for providing an uncorrected phase error signal (ϕ) having a value at ~~the~~ an instance the phase detector goes from the phase acquisition mode to the tracking mode (gear shift) of (ϕ_1);

an oscillator having an input;

a calculation circuit for calculating an offset adjustment value ($\Delta\phi$) which is equal to (α_1/α_2 -1) * ϕ_1, where (α_1) is a first PLL loop gain constant and (α_2) is a second PLL loop gain constant which is smaller in value than the first PLL loop gain constant (α_1);

a summing circuit coupled to the phase detector for adding the uncorrected phase error signal with ~~the~~ a phase error adjustment value and providing it as a summation circuit output signal; and

a multiplier circuit for multiplying the summation circuit output signal with either the first (α_1) or second (α_2) PLL loop gain constant and providing the result as a multiplier output signal that is provided to the input of the oscillator as a tuning word.

14. (Currently amended) A PLL synthesizer as defined in claim 13, wherein the ~~summing circuit adds the phase error adjustment value and the~~ multiplier multiplies the summation circuit output signal with the second PLL loop gain constant upon the PLL synthesizer moving from a phase/frequency acquisition mode to a tracking mode.

15. (Currently amended) A PLL synthesizer as defined in claim 14, wherein ~~the~~ a normalized loop gain (α_1/α_2) comprises a power-of-two value.

16. (Original) A PLL synthesizer as defined in claim 14, wherein the uncorrected phase error signal (ϕ) provided by the phase detector includes a reference phase (R_R), and a variable phase (R_V) and further comprising:

a reference register used to store the value of the reference phase (R_R), and the value of the variable phase (R_V) is loaded in the reference register in order to bring the uncorrected phase error equal to zero.

17. (Original) A PLL synthesizer as defined in claim 16, wherein a regular adjustment is performed using a frequency control word (FCW).